Transaction-Level Modeling with SystemC

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Currently employed at STMicroelectronics, Transactional-Level Modeling (TLM) puts forward a novel SoC design methodology beyond RTL with measured improvements of productivity and first time silicon success. The SystemC consortium has published the official TLM development kit in May 2005 to standardize this modeling technique. The library is flexible enough to model components and systems at many different levels of abstractions: from cycle-accurate to untimed models, and from bit-true behavior to floating-point algorithms. However, careful selection of the abstraction level and associated methodology is crucial to ensure practical gains for design teams. Transaction-Level Modeling with SystemC presents the formalized abstraction and related methodology defined at STMicroelectronics, and covers all major topics related to the Electronic System-Level (ESL) industry: - TLM modeling concepts
- Early embedded software development based on SoC virtual prototypes
- Functional verification using reference models
- Architecture analysis with mixed TLM and cycle accurate platforms
- Unifying TLM and RTL with platform automation tools Complementary to the book, open source code to put this approach into practice is available on several Internet sites as indicated in the first chapter.

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